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EXAMINER	
BUDD, PAUL A	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/821,432	WU ET AL.	
	Examiner	Art Unit	
	Paul A. Budd	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *13 Sept 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: the specification contains several typographical and/or grammatical errors. For example:

Page 8, line 3, change "fielel" to "field",

Appropriate correction is required.

Claim Objections

2. Claim 3 objected to because of the following informalities:

On line 3, change the phrase "parallel the" to "parallel to the"

Claim 15 objected to because of the following informalities:

On line 1, change the phrase "claim 15" to "claim 14".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, 5-8, 14-20, 22-25, 31-35, 50 and 51 are rejected under 35 U.S.C. 102 (b) as being anticipated by Kuroi el al (US Patent Pub 2002/0038901).

Regarding claim 1,

Kuroi teaches, a semiconductor device [Figures 1,2; 101] comprising:

a substrate [Fig. 4 and 5, 1] including a source [6] and drain [6], the source [6] having a first edge [Fig. 1, A2] and the drain [6] having a first edge [Fig. 1, A2];

a gate [5] between the source [6] and drain [6], the gate [5] having a first portion [Fig. 1, the intersection of line A2 and element 5]; and

a first deep trench structure [AR2, 9; adjacent to line A2] located under the first portion [Fig. 1, line A2 intersected with 5] of the gate [5] and proximate to the first edge [Fig. 1, A2] of the source [Fig. 1; 6; region AR2 to the left of element 5] and the first edge [Fig. 1, A2] of the drain [Fig. 1; 6; region AR2 to the right of element 5].

Regarding claim 2,

Kuroi teaches, the semiconductor device [Figures 1,2; 101] of claim 1 further comprising:

the source [Figs. 4 and 5, 6] having a second edge [Fig. 1, the complement line of line A2 being located above line A1] and the drain [6] having a second edge [Fig. 1, the complement line of line A2 being located above line A1];

the gate [5] having a second portion [Fig. 1, the complement line of line A2]; and

a second deep trench structure [AR2, 9, Fig. 1, the complement line of line A2 being located above line A1] located under the second portion [Fig. 1, Fig. 1, the complement line of line A2 being located above line A1 intersected with element 5] of the gate [5] and proximate to the second edge [Fig. 1, Fig. 1, the complement line of line A2 being located above line A1] of the source [6] and the

second edge [Fig. 1, Fig. 1, the complement line of line A2 being located above line A1] of the drain [6].

Regarding claim 3,

Kuroi teaches, the semiconductor device [Figures 1,2; 101] of claim 2 wherein the first edge [Fig. 1, A2] of the source [Fig. 4 and 5; 6] and drain [6] are approximately parallel to the second edge [Fig. 1, Fig. 1, the complement line of line A2 being located above line A1] of the source [6] and drain [6], and wherein the first [Fig. 1; A2 line] and second deep trench structures [AR2, 9, Fig. 1, the complement line of line A2 being located above line A1] are approximately parallel to the first [Fig. 1, A2] and second edges [Fig. 1, Fig. 1, the complement line of line A2 being located above line A1], respectively.

Regarding claim 5,

Kuroi teaches, the semiconductor device [Figures 1,2; 101] of claim 1 wherein the first deep trench structure [AR2, 9; adjacent to line A2] exhibits a geometry [Fig. 1, line A2] selected from the group consisting of a straight line [Fig. 1, line A2], an angled line, a broken line, and a combination thereof.

Regarding claim 6,

Kuroi teaches, the semiconductor device [Figures 1,2; 101] of claim 1 further comprising:

an outside edge [Fig. 1, intersection of a 'complement line to line B2' and the line A2] on the source [6];

an outside edge [Fig. 1, intersection of line B2 and line A2] on the drain [6]; and

the first deep trench structure [AR2, 9; adjacent to line A2] having a length extending at least from the outside edge of the source [6] to the outside edge of the drain [6] [Fig. 1, from line B2-A2 to the source side's 'complement line B2'-A2].

Regarding claim 7,

Kuroi teaches, "the semiconductor device [Figures 1,2; 101] of claim 1 wherein the first deep trench structure [AR2, 9; adjacent to line A2] is substantially filled in with a material selected from the group consisting of silicon dioxide, silicon nitride, silicon oxynitride, a high k material, and a combination thereof." [Page 5, paragraph 0070, "Thus the trench 2 is filled with silicon oxide films 9A and 9B ... The silicon oxide film 9 is a so-called trench isolation."]. [Page 6, paragraph 0088, "Further, instead of the silicon oxide film 9Ba, for example, a silicon oxynitride film, a PSG film, a BPSG film, an FSG film or the like may be used."]

Regarding claim 8,

Kuroi teaches, "the semiconductor device [Figures 1,2; 101] of claim 1 wherein the substrate [1] is made of a material selected from the group consisting of crystal silicon, polycrystalline silicon, amorphous silicon, germanium, diamond, silicon germanium, silicon carbide, gallium arsenic, indium phosphide, semiconductor on insulator, and a combination thereof." [Page 4, paragraph

0067, " As shown in FIGS. 1 to 7, the semiconductor device 101 comprises a semiconductor substrate formed of, e. g., P-type silicon crystal 1."]

Regarding claim 14,

Kuroi teaches, "the semiconductor device [Figures 1,2; 101] of claim 1 wherein the gate [5] includes a gate electrode [5A, 5B] and a gate dielectric [4]." [Page 5, paragraph 0072; "a gate insulating film 4 extends on the main surface 1S of the substrate 1 across the substantial center of the active region AR1 (see FIG. 1). The gate insulating film 4 is formed of a silicon oxide film ..."]. [Page 5, paragraph 0073; " A polysilicon film 5A having a film thickness of about 40nm to 70 nm and a tungsten silicide film 5B having a film thickness of about 50 nm to 100 nm are layered on the gate insulating film 4 ...].

Regarding claim 15,

Kuroi teaches, "the semiconductor device [Figures 1,2; 101] of claim 14 wherein the gate electrode [5A, 5B] is made of a material selected from the group consisting of doped polysilicon, metal, metal alloy, metal silicide, and a combination thereof ". [Page 5, paragraph 0073; " A polysilicon film 5A having a film thickness of about 40nm to 70 nm and a tungsten silicide film 5B having a film thickness of about 50 nm to 100 nm are layered on the gate insulating film 4 in this order, and the polysilicon film 5A and the tungsten silicide film 5B form a gate electrode 5."].

Regarding claim 16, 33,

Kuroi teaches, "the semiconductor device [Figures 1,2; 101] of claim 15 (or claim 31) wherein the gate dielectric [4] is made of a material selected from the group consisting of silicon oxide, silicon oxynitride, a high k material, and a combination thereof." [Page 5, paragraph 0072; "a gate insulating film 4 extends on the main surface 1S of the substrate 1 across the substantial center of the active region AR1 (see FIG. 1). The gate insulating film 4 is formed of a silicon oxide film ..."].

Regarding claim 17, 34,

Kuroi teaches, "the semiconductor device [Figures 1,2; 101] of claim 1 (or claim 18) wherein the first deep trench structure [2,9, line A2] extends around the entire device." [Fig. 1, region AR2].

Regarding claim 18,

Kuroi teaches, a semiconductor device [Figures 1,2; 101] comprising:

a substrate [1] including a source [6] and a drain [6], the source [6] having a first edge [Fig. 1, A2] and the drain [6] having a first edge [Fig. 1, A2];

a gate electrode [5] on the substrate [1] and between the source [6] and drain [6], a first portion [Fig. 1, A2] of the gate electrode [5] extending past the first edge [Fig. 1, A2] of the source [6] and the first edge of the drain [6];

a first deep trench structure [AR2, 9; adjacent to line A2] located under the first portion [line A2] of the gate electrode [5] and proximate to the first edge [line A2] of the source [6] and the first edge [line A2] of the drain [6].

Regarding claim 19,

Kuroi teaches, the semiconductor device [Figures 1,2; 101] of claim 18 further comprising:

the source [6] having a second edge [Fig. 1, the complement line of line A2 located above line A1] and the drain [6] having a second edge [Fig. 1, the complement line of line A2 located above line A1];

a second portion [Fig. 1, the complement line of line A2 located above line A1 intersecting element 5] of the gate electrode [5] extending past the second edge [Fig. 1, the complement line of line A2 located above line A1] of the source [6] and the second edge [Fig. 1, the complement line of line A2 located above line A1] of the drain [6];

a second deep trench structure [AR2, 9, along the complement line of line A2] located under the second portion [Fig. 1, the complement line of line A2 located above line A1 intersecting element 5] of the gate electrode [5] and proximate to the second edge [Fig. 1, the complement line of line A2] of the source [6] and the second edge [Fig. 1, the complement line of line A2] of the drain [6].

Regarding claim 20,

Kuroi teaches, the semiconductor device [Figures 1,2; 101] of claim 19 wherein the first edge [Fig. 1, A2] of the source [6] is

approximately parallel to the second edge [Fig. 1, the complement line of line A2] of the source [6], the first edge [Fig. 1, A2] of the drain [6] is

approximately parallel to the second edge [Fig. 1, the complement line of line A2] of the drain [6], the first deep trench structure [AR2, 9; adjacent to line A2] is approximately parallel to the first edges [line A2] and the second deep trench structure [AR2, 9, along the complement line of line A2] is approximately parallel to the second edges [the complement line of line A2 located above line A1].

Regarding claim 22,

Kuroi teaches, the semiconductor device [Figures 1,2; 101] of claim 18 wherein the first deep trench [AR2, 9; adjacent to line A2] exhibits a geometry [Fig. 1, A2] selected from the group consisting of a straight line [Fig. 1, A2], an angled line, a broken line, and a combination thereof.

Regarding claim 23,

Kuroi teaches, the semiconductor device [Figures 1,2; 101] of claim 18 further comprising:

an outside edge [Fig. 1, intersection of a 'complement line to line B2' and A2] on the source [6];

an outside edge [Fig. 1, intersection of line B2 and A2] on the drain [6]; and

the first deep trench [AR2, 9; adjacent to line A2] having a length extending at least from the outside edge of the source [6] to the outside edge of the drain [6] [Fig. 1, from line B2-A2 to the source side's 'complement line B2'-A2].

Regarding claim 24,

Kuroi teaches, the semiconductor device [Figures 1,2; 101] of claim 18 wherein the first deep trench structure [AR2, 9; adjacent to line A2] is substantially filled in with a material selected from the group consisting of silicon dioxide, silicon nitride, silicon oxynitride, a high k material, and a combination thereof. [Page 5, paragraph 0072; "a gate insulating film 4 extends on the main surface 1S of the substrate 1 across the substantial center of the active region AR1 (see FIG. 1). The gate insulating film 4 is formed of a silicon oxide film ..."].

Regarding claim 25,

Kuroi teaches, "the semiconductor device [Figures 1,2; 101] of claim 18 herein the substrate [1] is made of a material selected from the group consisting of crystal silicon, polycrystalline silicon, amorphous silicon, germanium, diamond, silicon germanium, silicon carbide, gallium arsenic, indium phosphide, semiconductor on insulator, and a combination thereof." [Page 4, paragraph 0067, " As shown in FIGS. 1 to 7, the semiconductor device 101 comprises a semiconductor substrate formed of, e. g., P-type silicon crystal 1."]

Regarding claim 31,

Kuroi teaches, the semiconductor device [Figures 1,2; 101] of claim 18 further comprising:

a gate dielectric [Fig. 2; 4] adjacent to the gate electrode [Fig. 2; 5A, 5B].

Regarding claim 32,

Kuroi teaches, "the semiconductor device [Figures 1,2; 101] of claim 18 wherein the gate electrode [5A, 5B] is made of a material selected from the group consisting of doped polysilicon, metal, metal alloy, metal silicide, and a combination thereof ". [Page 5, paragraph 0073; " A polysilicon film 5A having a film thickness of about 40nm to 70 nm and a tungsten silicide film 5B having a film thickness of about 50 nm to 100 nm are layered on the gate insulating film 4 in this order, and the polysilicon film 5A and the tungsten silicide film 5B form a gate electrode 5."].

Regarding claim 35,

Kuroi teaches, "a semiconductor device [Figures 1,2; 101] comprising:

a substrate [Fig. 4 and 5, 1] having a source [6] and a drain [6], the source [6] and the drain [6] having widths that are substantially equal [see Fig. 1] and each having a first edge [Fig. 1, A2] substantially located along a common line [A1] on the substrate [1];

a gate electrode [Fig. 2; 5A, 5B] on the substrate [1] and between the source [6] and the drain [6], the gate electrode [5A, 5B] having a first portion [Fig. 1, the intersection of line A2 and element 5] extending past the first edge [Fig. 1, A2] of the source [6] and the first edge [Fig. 1, A2] of the drain [6];

a first deep trench structure [AR2, 9, adjacent to line A2] located under the first portion [Fig. 1, the intersection of line A2 and element 5] of the gate electrode [5A, 5B], the first deep trench structure [AR2, 9, adjacent to line A2] parallel to the common line [Fig. 1, A1] on the substrate [1] and proximate to the

first edge [Fig. 1, A2] of the source [6] and the first edge [Fig. 1, A2] of the drain [6].

Regarding claim 50,

Kuroi teaches, a semiconductor device [Figures 1,2; 101] comprising:

a substrate [1] including a source [6] and a drain [6], the source [6] having a first edge [Fig. 1, A2] and the drain [6] having a first edge [Fig. 1, line A2];

a gate electrode [5A, 5B] on the substrate [1] and between the source [6] and drain [6], a first portion [Fig. 1, line A2] of the gate electrode [5A, 5B] extending past the first edge [Fig. 1, A2] of the source [6] and the first edge [Fig. 1, A2] of the drain [6];

a current channel [Fig. 1, intersection of element 5 and line A2] located in a region where the gate electrode [5A, 5B] extends beyond the first edge [Fig. 1, line A2] of the source [6] and the first edge [Fig. 1, line A2] of the drain [6], the current channel allowing a leakage current to flow in the device [Figures 1,2; 101];

a first deep trench structure [Fig. 1; AR2, 9; adjacent to line A2] located under the first portion [Fig. 1, line A2 intersecting element 5] of the gate electrode [5A, 5B] and proximate to the first edge [Fig. 1, line A2] of the source [6] and the first edge [Fig. 1, line A2] of the drain [6], whereby the first deep trench structure [Fig. 1; AR2, 9; adjacent to line A2] is located close enough to the first edge [Fig. 1, line A2] of the source [6] and the first edge [Fig. 1, line A2] of the drain [6] to substantially eliminate the leakage current flow through the current channel.

[Placing a thick oxide region under the gate on the outside edge (first portion) of the device will substantially reduce any edge leakage currents, in the transistor's on or off state. When the parasitic device defined by this claim is in saturation ("high enough voltage is applied to the gate") the device current is inversely proportional to the trench thickness as given by the equation Ids={(carrier mobility) times (the capacitance of the oxide) times (the width of the device) times (the square of Gate potential minus the threshold) divided by two times the channel length)}. The capacitance of the oxide, for this parasitic device, is inversely proportional to the trench thickness. Therefore, creating a thick oxide (the deep trench) in this edge region will reduce undesirable parasitic device currents. This is one motivation for using LOCOS or trench isolation as a general rule. If the parasitic transistor is operated in the linear region, as opposed to saturation the current is still inversely proportional to the deep trench thickness. The reference, Kuroi, makes use of this knowledge when he states on page 3, paragraph 0041 "In the method of the sixth aspect of the present invention, in the oxidation step (e), the edge portion of the oxide film is made thicker than the initial state (in step (b)). Therefore, ... with the thicker portion (edge portion) of the oxide film, it is possible to avoid sag near the opening edge of the trench. Accordingly, it is possible to suppress formation of parasitic elements due to presence of the sag and reduce the problems in operation of the semiconductor device.] .

Regarding claim 51,

Kuroi teaches, a method of manufacturing a microelectronic device [Figures 1,2; 101], comprising:

forming a substrate [Fig. 1,2; 1; Page 4, paragraph 0067, " As shown in FIGS. 1 to 7, the semiconductor device 101 comprises a semiconductor substrate formed of, e. g., P-type silicon crystal 1."] including a source [6; Page 5, paragraphs 0074 and 0075] and a drain [6; Page 5, paragraphs 0074 and 0075];

forming a gate [Fig. 1,2; 5; Page 5 paragraphs 0072 and 0073] between the source [6] and drain [6]; and

forming a deep trench structure [Fig. 1,2; 9; Page 4-5 paragraphs 0067, 0068 ,0069 ,0070] under a portion of the gate [5] and proximate to an edge of the source [6] and drain [6].

4. Claims 1-8,10-12, 14-25, 27-29,31-40, 42-44, and 46-51 are rejected under 35 U.S.C. 102 (b) as being anticipated by Iwata el al (US Patent Pub 2003/0107103).

Regarding claim 1,

Iwata teaches, a semiconductor device [Figures 1,2,3,4; 2] comprising:

a substrate [Fig. 1,2,3,4; 11] including a source [20] and drain [21], the source [20] having a first edge [Fig. 1, the horizontal line just above the line marked by element 25; also see Fig. 4 the far left hand side] and the drain [21] having a first edge [Fig. 1, the horizontal line just above the line marked by 25];

a gate [Fig. 2; 24,25,26,29] between the source [20] and drain [21], the gate [24,25,26,29] having a first portion [Fig. 1, the line just above 25]; and

a first deep trench structure [Fig. 4 the far left hand side, 22] located under the first portion [Fig. 1, the line just above 25] of the gate [Fig. 4, 24,25,26,29] and proximate to the first edge [Fig. 1, the line just above 25] of the source [20] and the first edge [Fig. 1, the line just above 25] of the drain [21].

Regarding claim 2,

Iwata teaches, the semiconductor device [Figures 1,2,3,4; 2] of claim 1 further comprising:

the source [20] having a second edge [Fig. 1, a line halfway between A-A' and B-B'; or Fig. 4, a line drawn vertically through 23 in the middle of the figure] and the drain [21] having a second edge [Fig. 1, Fig. 4 see above];

the gate [24,25,26,29] having a second portion [Fig. 1, Fig. 4 see above]; and

a second deep trench structure [Figure 4, element labeled 22 towards the right of center] located under the second portion of the gate [24,25,26,29] and proximate to the second edge [Fig. 4 center of figure] of the source [20] and the second edge [Fig. 4 center of figure] of the drain [21].

Regarding claims 3, 20,

Iwata teaches, the semiconductor device [Figures 1,2,3,4; 2] of claim 2 (or claim 19) wherein the first edge [Fig. 1, the line just above 25] of the source [20] and drain [21] are approximately parallel to the second edge [Fig. 1, a line halfway between A-A' and B-B'; or Fig. 4, a line drawn vertically through 23 in the middle of the figure] of the source [20] and drain [21], and wherein the first [Fig. 1, the

horizontal line marked by 25] and second deep trench structure [Figure 4, element labeled 22] are approximately parallel [see Figures 1 and 4] to the first and second edges , respectively.

Regarding claim 4,

Iwata teaches, the semiconductor device [Figures 1,2,3,4; 2] of claim 1 wherein the first deep trench structure [Fig. 4 the far left hand side of the figure, 22] has a depth greater than 0.5 um [Page 5, paragraph 0088; "A depth of the deep element isolation region ... that may be, for example, 0.3 to 2 um."].

Regarding claim 5,

Iwata teaches, the semiconductor device [Figures 1,2,3,4; 2] of claim 1 wherein the first deep trench structure [Figure 1, 22; Fig. 4 the far left hand side of the figure, 22] exhibits a geometry selected from the group consisting of a straight line [Figure 1, 22 along line A2], an angled line, a broken line, and a combination thereof.

Regarding claims 6, 23, 38,

Iwata teaches, the semiconductor device [Figures 1,2,3,4; 2] of claim 1 further comprising:

an outside edge [Fig. 1, lower right hand side of source] on the source [20];

an outside edge [Fig. 1, lower corner of the drain near lower middle of the figure] on the drain [21]; and

the first deep trench structure [Fig. 1, 22 at the very bottom of the figure] having a length extending at least from the outside edge of the source [20] to the outside edge of the drain [21].

Regarding claims 7,24,39,

Iwata teaches, the semiconductor device [Figures 1,2,3,4; 2] of claim 1 (and claim 18 and claim 35) wherein the first deep trench structure [Fig. 1, 22 at the very bottom of the figure] is substantially filled in with a material selected from the group consisting of silicon dioxide, silicon nitride, silicon oxynitride, a high k material, and a combination thereof. [Page 5, paragraph 0083, "Materials of the trench-filling film 415 may include insulators such as oxide and silicon nitride films and conducting films such as amorphous silicon and polysilicon"]

Regarding claims 8, 25, 40,

Iwata teaches, the semiconductor device [Figures 1,2,3,4; 2] of claim 1 (or claim 18 or claim 35) wherein the substrate [11] is made of a material selected from the group consisting of crystal silicon, polycrystalline silicon, amorphous silicon, germanium, diamond, silicon germanium, silicon carbide, gallium arsenic, indium phosphide, semiconductor on insulator, and a combination thereof." [Page 4, paragraph 0072; "Material for a semiconductor substrate used in the present invention is not particularly limited, but silicon is rather preferable."]

Regarding claims 10, 27, 42,

Iwata teaches, the semiconductor device [Figures 1,2,3,4; 2] of claim 1 (or claim 18 or claim 35) comprising:

a neighboring semiconductor device [Figures 1,2,3,4; 1]; and

a first shallow trench isolation structure [Fig. 1 center of figure, 23] located between the semiconductor device [Figures 1,2,3,4; 2] and the neighboring semiconductor device [Figures 1,2,3,4; 1].

Regarding claims 11, 28, 43,

Iwata teaches, the semiconductor device [Figures 1,2,3,4; 2] of claim 10 (or claim 27 or claim 42) further comprising:

a second shallow trench isolation structure [Fig. 3; 23 (not the center 23 but the 23s to the right hand side)] [also see Fig. 4, center of figure, 23] adjacent to the drain [21] wherein the drain [21] is situated between the first shallow trench isolation structure [Fig. 1; center 23] and the second shallow trench isolation structure [Fig. 3; 23] [also see Fig. 4, center of figure, 23].

Regarding claim 12, 29, 44,

Iwata teaches, the semiconductor device [Figures 1,2,3,4; 2] of claim 11 (or claim 28 or claim 43) wherein the gate [24,25,26,29] is extended to partially overlay [Figure 1] the second shallow trench isolation structure [Fig. 1; 23] [also see Fig. 4; 25 over 23].

Regarding claim 14,

Iwata teaches, "the semiconductor device [Figures 1,2,3,4; 2] of claim 1 wherein the gate [24,25,26,29] includes a gate electrode [25] and a gate dielectric [24]."

Regarding claims 15, 32, 47,

Iwata teaches, "the semiconductor device [Figures 1,2,3,4; 2] of claim 14 (or claim 18 or claim 35) wherein the gate electrode [25] is made of a material selected from the group consisting of doped polysilicon, metal, metal alloy, metal silicide, and a combination thereof ". [Page 7, paragraph 0102; "If silicon substrates are used, the gate electrode 25 is made of silicon films such as polysilicon and single crystal silicon. Other metal films made of aluminum or copper may be used"].

Regarding claims 16, 33, 48,

Iwata teaches, "the semiconductor device [Figures 1,2,3,4; 2] of claim 15 (or claim 31 or claim 46) wherein the gate dielectric [24] is made of a material selected from the group consisting of silicon oxide, silicon oxynitride, a high k material, and a combination thereof." [Page 7, paragraph 0101; "Materials of the insulating film 24 are not specifically limited as long as they have the insulating property. If silicon substrates are used, silicon oxide films, silicon nitride films, or laminated products thereof are applicable.].

Regarding claims 17, 34, 49,

Iwata teaches, "the semiconductor device [Figures 1,2,3,4; 2] of claim 1 (or claim 18 or claim 35) wherein the first deep trench structure [Fig. 1, 22 at the very bottom of the figure] extends around the entire device." [Fig. 1, 22].

Regarding claim 18,

Iwata teaches, a semiconductor device [Figures 1,2,3,4; 2] comprising:

a substrate [11] including a source [20] and a drain [21], the source [20] having a first edge [Fig. 1, the line just above the line marked by 25] and the drain [21] having a first edge [Fig. 1, the line just above the line marked by 25];

a gate electrode [25] on the substrate [11] and between the source [20] and drain [21], a first portion [Fig. 1, the line just above 25; also see Fig. 4, left hand side of figure] of the gate electrode [25] extending past the first edge [Fig. 1, the line just above 25; also Fig. 4 left hand side of figure, 25 over 23] of the source [20] and the first edge of the drain [21];

a first deep trench structure [Fig. 4 the far left hand side of the figure, 22] located under the first portion [Fig. 1, the line marked by 25; also see Fig. 4, the far left hand side of the figure] of the gate electrode [25] and proximate to the first edge [Fig. 1, the line just above the line marked by 25] of the source [20] and the first edge [Fig. 1, the line just above 25] of the drain [21].

Regarding claim 19,

Iwata teaches, the semiconductor device [Figures 1,2,3,4; 2] of claim 18 further comprising:

the source [20] having a second edge [Fig. 1, a line halfway between A-A' and B-B'; Fig. 4, a line drawn vertically through 23 in the middle of the figure] and the drain [21] having a second edge [Fig. 1, Fig. 4 see above];

a second portion [Fig. 1, Fig. 4 see above] of the gate electrode [25] extending past the second edge [Fig. 1, Fig. 4 see above] of the source [20] and the second edge [Fig. 1, Fig. 4 see above] of the drain [21];

a second deep trench structure [Figure 4, the element labeled 22 towards the right of the figure] located under the second portion [Fig. 4, 25] of the gate electrode [25] and proximate to the second edge [Fig. 4 center of figure] of the source [20] and the second edge [Fig. 4 center of figure] of the drain [21].

Regarding claims 21, 37,

Iwata teaches, the semiconductor device [Figures 1,2,3,4; 2] of claim 18 (or claim 35) wherein the first deep trench structure [Fig. 4, the far left hand side of figure, 22] has a depth greater than 0.5 um [Page 5, paragraph 0088; "A depth of the deep element isolation region ... that may be, for example, 0.3 to 2 um."].

Regarding claim 22,

Iwata teaches, the semiconductor device [Figures 1,2,3,4; 2] of claim 18 wherein the first deep trench [Fig 1, 22; Fig. 4 left hand side, 22] exhibits a geometry selected from the group consisting of a straight line [Fig. 1, 22 bottom of figure], an angled line, a broken line, and a combination thereof.

Regarding claims 31, 46,

Iwata teaches, the semiconductor device [Figures 1,2,3,4; 2] of claim 18 (or claim 35) further comprising:

a gate dielectric [Fig.2; 24] adjacent to the gate electrode [Fig.2; 25].

Regarding claim 35,

Iwata teaches, "a semiconductor device [Figures 1,2,3,4; 2] comprising:

a substrate [11] having a source [20] and a drain [21], the source [20] and the drain [21] having widths that are substantially equal [see Fig. 1] and each

having a first edge [Fig. 1, the line just above the line marked by 25] substantially located along a common line on the substrate [11];

a gate electrode [25] on the substrate [11] and between the source [20] and the drain [21], the gate electrode [25] having a first portion [Fig. 1, the line just above the line marked by 25] extending past the first edge [Fig. 1, the line just above the line marked by 25] of the source [20] and the first edge [Fig. 1, the line just above the line marked by 25] of the drain [21];

a first deep trench structure [Fig. 4 the far left hand side of figure, 22] located under the first portion [Fig. 1, the line marked by 25; also see Fig. 4 the far left hand side of figure] of the gate electrode [25], the first deep trench structure [22] parallel to the common line [Fig. 1, the line just above the line marked by 25] on the substrate [11] and proximate to the first edge [Fig. 1, the line marked by 25; also see Fig. 4, left hand side of figure] of the source [20] and the first edge [Fig. 1, the line just above the line marked by 25] of the drain [21].

Regarding claim 36,

See explanation above for claim 19. Iwata teaches "the source and drain having a second edge parallel to their respective first edges" [Fig. 1, note parallel edges of the lines identified above].

Regarding claim 50,

Iwata teaches, a semiconductor device [Figures 1,2,3,4; 2] comprising:

a substrate [11] including a source [20] and a drain [21], the source [20] having a first edge [Fig. 1, the line just above the line marked by 25] and the drain [21] having a first edge [Fig. 1, the line just above the line marked by 25];

a gate electrode [25] on the substrate [11] and between the source [20] and drain [21], a first portion [Fig. 1, the line just above the line marked by 25] of the gate electrode [25] extending past the first edge [Fig. 1, the line just above the line marked by 25] of the source [20] and the first edge [Fig. 1, the line just above the line marked by 25] of the drain [21];

a current channel [Fig. 1, the line marked by 25] located in a region where the gate electrode [25] extends beyond the first edge [Fig. 1, the line just above the line marked by 25] of the source [20] and the first edge [Fig. 1, the line just above the line marked by 25] of the drain [21], the current channel allowing a leakage current to flow in the device [Figures 1,2,3,4; 2];

a first deep trench structure [Fig. 4 the far left hand side of figure, 22] located under the first portion [Fig. 1, the line marked by 25] of the gate electrode [25] and proximate to the first edge [Fig. 1, the line just above the line marked by 25] of the source [20] and the first edge [Fig. 1, the line just above the line marked by 25] of the drain [21], whereby the first deep trench structure [Fig. 4 the far left hand side of figure, 22] is located close enough to the first edge [Fig. 1, the line just above the line marked by 25] of the source [21] and the first edge [Fig. 1, the line just above the line marked by 25] of the drain [21] to substantially eliminate the leakage current flow through the current channel. [The reference,

Iwata, states the benefits on page 8, paragraph 0114, " The semiconductor device is provided with both a deep element isolation region 22 with an approximately constant width and a shallow element isolation region 23 made of STI as the element isolation region, and the shallow element isolation region 23 is free from remarkable bird's beak like isolation oxide. This enables prevention of off leakage failure of PMOS 2 due to stress caused by bird's beak, and minimizes margin between elements or inter-elements."].

Regarding claim 51,

Iwata teaches, a method of manufacturing a microelectronic device [Figures 1,2,3,4; 2], comprising:

forming a substrate [Fig. 2; 11; Page 4, paragraph 0074, "As shown in FIG. 2, the semiconductor device in the first embodiment of the present invention has an N-type deep well region 12 and a P-type deep well region 13 formed inside a P-type semiconductor substrate"] including a source [20; Page 7, paragraphs 0106-0110] and a drain [21; Page 7, paragraphs 0106-0110];

forming a gate [Fig. 2; 25; Page 7, paragraphs 0100-0103] between the source [20] and drain [21]; and

forming a deep trench structure [Fig. 1,2; 22; Page 4-5 paragraphs 0082-0088] under a portion of the gate [25] and proximate to an edge of the source [20] and drain [21].

5. Claim 50 is rejected under 35 U.S.C. 102 (b) as being anticipated by Joyner el al (US Patent 6,114,741).

Regarding claim 50,

Joyner teaches, a semiconductor device [Fig. 3] comprising:

a substrate [Fig. 2, 10] including a source [Fig. 2, S] and a drain [Fig. 2, D], the source [S] having a first edge [Fig. 3, horizontal line marked by 32] and the drain [D] having a first edge [Fig. 3, horizontal line marked by 32];

a gate electrode [Fig. 2,3; 26] on the substrate [10] and between the source [S] and drain [D], a first portion [Fig. 3, horizontal line marked by 32] of the gate electrode [26] extending past the first edge [Fig. 3, horizontal line marked by 32] of the source [S] and the first edge [Fig. 3, horizontal line marked by 32] of the drain [D];

a current channel [Fig. 3, horizontal line marked by 32 intersected with 26] located in a region where the gate electrode [26] extends beyond the first edge [Fig. 3, horizontal line marked by 32] of the source [S] and the first edge [Fig. 3, horizontal line marked by 32] of the drain [D], the current channel allowing a leakage current to flow in the device [Fig. 3];

a first deep trench structure [Figures 3; 22 adjacent to the horizontal line marked by 32] located under the first portion [Fig. 3, horizontal line marked by 32 intersected with 26] of the gate electrode [26] and proximate to the first edge [Fig. 3, horizontal line marked by 32] of the source [S] and the first edge [Fig. 3, horizontal line marked by 32] of the drain [D], whereby the first deep trench

structure [Fig. 2,3; 22 adjacent to the horizontal line marked by 32] is located close enough to the first edge [Fig. 3, horizontal line marked by 32] of the source [S] and the first edge [Fig. 3, horizontal line marked by 32] of the drain [D] to substantially eliminate the leakage current flow through the current channel [Page 5, paragraph 5, lines 52-55, The portion of refill oxide 22 that covers all or a portion of top corner 30 and top corner 32 prevents the formation of a parasitic transistor with a threshold voltage Vt, that is less than the threshold voltage Vt of the main transistor.].

6. Claims 1,9,18,26,35,41 are rejected under 35 U.S.C. 102(b) as being anticipated by Hara et al (US Pat Pub 2004/0029355).

Regarding claim 1,

Hara teaches, a semiconductor device [Fig. 4A,4B] comprising:

a substrate [Fig. 4A ,4B; 1] including a source [13] and drain [13], the source [13] having a first edge [Fig. 4B, the lower horizontal line intersecting the gate 12] and the drain [13] having a first edge [Fig. 4B, the lower horizontal line intersecting the gate 12];

a gate [12] between the source [13] and drain [13], the gate [12] having a first portion [Fig. 4B, the lower horizontal line intersecting the gate 12]; and

a first deep trench structure [Fig. 4B, the lower horizontal line intersecting the gate 12, element 7] located under the first portion [Fig. 4B, the lower horizontal line intersecting the gate 12] of the gate [12] and proximate to the first

edge [Fig. 4B, the lower horizontal line intersecting the gate 12] of the source [13] and the first edge [Fig. 4B, the lower horizontal line intersecting the gate 12] of the drain [13].

Regarding claims 9, 26, 41,

Hara teaches, the semiconductor device [Fig. 4A, 4B] of claim 1 (or 18 or 35) wherein the device includes a strained [Fig. 4A, 3] MOS structure [Page 4, paragraph 0062; "Note that a semiconductor device including an Si layer and a SiGe layer (i.e., a strained SiGe layer) grown on the Si layer will be described as a semiconductor device including a SiGe layer."].

Regarding claim 18,

Hara teaches, a semiconductor device [Fig. 4A,4B] comprising:

a substrate [Fig. 4A,4B; 1] including a source [13] and a drain [13], the source [13] having a first edge [Fig. 4B, the lower horizontal line intersecting the gate 12] and the drain [13] having a first edge [Fig. 4B, the lower horizontal line intersecting the gate 12];

a gate electrode [12] on the substrate [1] and between the source [13] and drain [13], a first portion [Fig. 4B, the lower horizontal line intersecting the gate 12] of the gate electrode [12] extending past [see Fig. 4B] the first edge [Fig. 4B, the lower horizontal line intersecting the gate 12] of the source [13] and the first edge of the drain [13];

a first deep trench structure [Fig. 4B, the lower horizontal line intersecting the gate 12, element 7] located under the first portion [Fig. 4B, the lower

horizontal line intersecting the gate 12] of the gate electrode [12] and proximate to the first edge [Fig. 4B, the lower horizontal line intersecting the gate 12] of the source [13] and the first edge [Fig. 4B, the lower horizontal line intersecting the gate 12] of the drain [13].

Regarding claim 35,

Hara teaches, "a semiconductor device comprising:

a substrate [Fig. 4A,4B; 1] having a source [13] and a drain [13], the source [13] and the drain [13] having widths that are substantially equal [See Fig. 4B] and each having a first edge [Fig. 4B, the lower horizontal line intersecting the gate 12] substantially located along a common line on the substrate [1];

a gate electrode [12] on the substrate [1] and between the source [13] and the drain [13], the gate electrode [12] having a first portion [Fig. 4B, the lower horizontal line intersecting the gate 12] extending past the first edge [Fig. 4B, the lower horizontal line intersecting the gate 12] of the source [13] and the first edge [Fig. 4B, the lower horizontal line intersecting the gate 12] of the drain [13];

a first deep trench structure [Fig. 4B, the lower horizontal line intersecting the gate 12, element 7] located under the first portion [Fig. 4B, the lower horizontal line intersecting the gate 12] of the gate electrode [12], the first deep trench structure [Fig. 4B, the lower horizontal line intersecting the gate 12, element 7] parallel to the common line [Fig. 4B, the lower horizontal line intersecting the gate 12] on the substrate [1] and proximate to the first edge [Fig. 4B, the lower horizontal line intersecting the gate 12] of the source [13] and the

first edge [Fig. 4B, the lower horizontal line intersecting the gate 12] of the drain [13].

7. Claims 1,13,18,30,35,45, are rejected under 35 U.S.C. 102(b) as being anticipated by Kotani (US Pat Pub 2001/0035774).

Regarding claim 1,

Kotani teaches, a semiconductor device [Fig. 1, 1] comprising:

a substrate [10] including a source [Fig. 1, 15] and drain [Fig. 1, 16], the source [15] having a first edge [Fig. 2, the horizontal line just above the edge marked by 40] and the drain [16] having a first edge [Fig. 2, the horizontal line just above the edge marked by 40];

a gate [Fig 1,2; 19] between the source [15] and drain [16], the gate [19] having a first portion [Fig. 2, the horizontal line just above the edge marked by 40 intersected with 19]; and

a first deep trench structure [Fig. 1,2; element 13 adjacent to the horizontal line just above the edge marked by 40] located under the first portion [Fig. 2, the horizontal line just above the edge marked by 40 intersected with 19] of the gate [19] and proximate to the first edge [Fig. 2, the horizontal line just above the edge marked by 40] of the source [15] and the first edge [Fig. 2, the horizontal line just above the edge marked by 40] of the drain [16].

Regarding claims 13,30,45,

Kotani teaches, the semiconductor device [Fig. 1, 1] of claim 1 (or 18 or 35) further comprising;

a body contact feature [Fig. 2; 40a, 44,45] adjacent to the source [15]. [Page 3, paragraph 0040; "A body contact 44 is formed in the extended region 40a and a body contact portion 45 is made up of the extended region 40a and the body contact 44.]

Regarding claim 18,

Kotani teaches, a semiconductor device [Fig. 1, 1] comprising:

a substrate [10] including a source [Fig. 1, 15] and a drain [Fig. 1, 16], the source [15] having a first edge [Fig. 2, the horizontal line just above the edge marked by 40] and the drain [16] having a first edge [Fig. 2, the horizontal line just above the edge marked by 40];

a gate electrode [19] on the substrate [10] and between the source [15] and drain [16], a first portion [Fig. 2, the horizontal line just above the edge marked by 40 intersected with 19] of the gate electrode [19] extending past [See Fig. 2] the first edge [Fig. 2, the horizontal line just above the edge marked by 40 intersected with 19] of the source [15] and the first edge [Fig. 2, the horizontal line just above the edge marked by 40 intersected with 19] of the drain [16];

a first deep trench structure [Fig. 1,2; element 13 adjacent to the horizontal line just above the edge marked by 40] located under the first portion [Fig. 2, the horizontal line just above the edge marked by 40 intersected with 19] of the gate electrode [19] and proximate to the first edge [Fig. 2, the horizontal

line just above the edge marked by 40] of the source [15] and the first edge [Fig. 2, the horizontal line just above the edge marked by 40] of the drain [16].

Regarding claim 35,

Kotani teaches, "a semiconductor device comprising:

a substrate [10] having a source [15] and a drain [16], the source [15] and the drain [16] having widths that are substantially equal [See Fig. 2] and each having a first edge [Fig. 2, the horizontal line just above the edge marked by 40] substantially located along a common line on the substrate [10];

a gate electrode [19] on the substrate [10] and between the source [15] and the drain [16], the gate electrode [19] having a first portion [Fig. 2, the horizontal line just above the edge marked by 40 intersected with 19] extending past the first edge [Fig. 2, the horizontal line just above the edge marked by 40] of the source [15] and the first edge [Fig. 2, the horizontal line just above the edge marked by 40] of the drain [16];

a first deep trench structure [Fig. 1,2; element 13 adjacent to the horizontal line just above the edge marked by 40] located under the first portion [Fig. 2, the horizontal line just above the edge marked by 40 intersected with 19] of the gate electrode [19], the first deep trench structure [Fig. 1,2; element 13 adjacent to the horizontal line just above the edge marked by 40] parallel to the common line [See Fig. 1] on the substrate [10] and proximate to the first edge [Fig. 2, the horizontal line just above the edge marked by 40] of the source [15]

and the first edge [Fig. 2, the horizontal line just above the edge marked by 40] of the drain [16].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul A. Budd whose telephone number is 571-272-1664. The examiner can normally be reached on Monday to Friday 8:30 to 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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